ity of unidirectional point-to-point buses connect, the arbitration logic for granting each of the bus elements access to the at least one other bus element through the central unit one at a time based upon the requests from the bus elements.

REMARKS

Reconsidered and reexamination are respectfully requested in the identified patent application.

The Examiner rejected claims 1-29 under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter of Applicant's invention.

Applicants have amended independent claim 1 to recite "a plurality of bus elements, with each of the plurality making a request for access to at least one other bus element". Thus, applicants have deleted "selectively". Applicants maintain that as amended, claim 1, and dependant claims 2-29 now particularly point out and distinctly claim the subject matter of their invention under 35 U.S.C. §112, second paragraph and thus the rejection has been overcome.

The Examiner rejected claims 1-19, 30-35 and 37-39 under 35 U.S.C. §103 as being unpatentable over Rodiger et al. in view of Culler.

Applicant's claims 1-19, 30-35 and 37-39 are patentably distinct over the cited references. Applicant's claim 1 as amended, recites ... a plurality of bus elements, with each of the plurality of bus elements making requests for access to at least one other bus element...

The Examiner states that the references "fails to expressly teach the limitation of one bus element making a request for access to at least one other bus element". Further, the Examiner's specific reasons why one skilled in the art would be motivated to apply the teachings of Rodiger and Culler does not address the basis of applicants' invention. The Examiner states that "it would be obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Rodiger to include processor to processor communication...because it is well within the skill of an ordinary person to realize that outputs from a bus can be coupled to a memory and to it's associated processor (Culler teaches that in Fig. 6, elements 544, 548)". Applicants submit that Culler describes a bus arbitration system in which if a processor unit is denied access to the

system bus, and if there is no current conflict in requesting the processor unit's associated local memory, then a request to access the associated local memory, rather than the system bus, is granted. Applicants claim 1 recites on the other hand that the buses are coupled to the central unit via uni-directional buses (see the specification page 6 and claim 1 sections c and d). Therefore, claim 1 requires a unidirectional point-to-point connection to the target bus, rather than through the associated memory as in Culler, and thus has improved access to a target element.

Thus, claim 1 which further recites ... a first plurality of unidirectional point-to-point buses for coupling in a first direction the bus elements to the central unit bus inputs ..., nor ... a second plurality of unidirectional point-to-point buses for coupling in a second direction each output of the central unit to a respective bus element... is neither described nor suggested by the combination of cited references.

The legal standard to be used when evaluating a claim under section 103 is to look at the teachings of the prior art as a whole for what they fairly teach, and neither the reference's general nor specific teachings may be ignored. The prior art must not only disclose each element of

the claim, but must also provide a suggestion or incentive to make the combination made by the inventor. Therefore, applicant's claim 1 is patentably distinct over the references since neither Rodiger nor Rodiger in combination with Culler describe or suggest the above mentioned claimed combination of unidirectional point-to-point buses coupled to a central unit.

Applicant's claims 2-19 are patentably distinct over the cited references for similar reasons as given above with reference to the independent claim upon which they are based.

Applicants maintain that claims 2-4 further limit claim 1 and are not simply a matter of design choice. Each of the three mentioned circuits, the state machine in claim 2, the OR gate in claim 3 and the multiplexer in claim 4, add further patentably distinct limitations to claim 1. For example, the state machine called for in claim 2 (see FIG.s 2 and 3, item 42) "stores the output for one cycle before providing it at it's output". (see specification page 9, Line 24-25). The OR gate called for in claim 3 (see FIG. 2, items 37 and 41) and the multiplexer called for in claim 4 (see FIG. 3, items 37 and 41) along with the logic element 50 provide alternative techniques to combine the point-to-

point signals (See page 5 lines 21-25 for the OR gate for example).

Similarly, applicants maintain that claims 5-19 provide patentably distinct features to Applicants claim 1 and are therefore also allowable over the cited references.

Applicant's claim 30 was rejected by the Examiner for the same reasons as claim 1. Claim 30 recites ... a plurality of first uni-directional point-to-point buses, with one bus coupling each of the central processing units to an input of the combining logic...a plurality of second uni-directional point-to-point buses coupling the output of the combining logic to the central processing units ... plus a ...plurality of central processing units... and ...a shared memory... plus a ...memory controller... Therefore, Applicants maintain that claim 30 is patentably distinct over the cited references for similar reasons to those given above with reference to claim 1.

Applicants maintain that claims 31-32 further limit claim 30 and are not simply a matter of design choice. Each of the mentioned circuits, the combining logic in claim 31 and the multiplexer in claim 32, add further patentably distinct limitations to claim 30. The combining logic called for in claim 31 and the multiplexer called for in claim 32 provide alternative techniques to combine the

point-to-point signals. Therefore the applicant's believe that the Examiner's rejection is improper and should be removed.

Applicants maintain that method claim 33 is patentably distinct over the cited references because claim 33 recites ...coupling each of the bus elements to a central unit with a separate first uni-directional bus... As explained above with reference to claim 1, the cited references do not describe nor suggest the claimed combination of features.

Applicants maintain that dependent claims 34 and 35 are allowable as further limitations on claim 33 above, since claim 34 recites ...a plurality of central processing units and a shared memory. Claim 35 recites the method of ...selecting between the inputs on the first buses...and the bus from the memory.

Applicants maintain that dependent claims 37-39 add further patentably distinct limitations to the claims above, and are therefore allowable. Claim 37 limits claim 2 by providing an alternative technique to combine the point-to-point signals, namely a latch. Claims 38 and 39 limits claim 5 and 1 in a similar fashion and are therefore add patentably distinct limitations.

Applicants note that the Examiner did not reject claims 20-29 over the prior art, and objected to claim 36 as being dependant on a rejected base claim.

Applicants submit that in view of the above amendment and remarks, that claims 1-35 and 37-39 are patentably distinct over the references.

Therefore, reconsideration and re-examination of this application is respectfully requested since the amendment places the application in condition for allowance or better form for appeal by materially reducing the issues on appeal.

Respectfully submitted,

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